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09/866,092	05/23/2001	Mark Thomas McCormack	6136/54242 (25916-217)	5484

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/866,092	MCCORMACK ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-24,26-34 and 36-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-24,26-34 and 36-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/17/06* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the applicant's arguments in the appeal brief filed 1/03/07, a new non-final rejection with new prior art is presented below.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first via extends from said first substrate surface to said second substrate surface (claim 20) must be shown or the feature(s) canceled from the claim(s). The figures (see, for example, FIG. 9) show a first via passing through said first dielectric layer that resides above a polymeric circuit substrate comprising the core of said multi-layer printed circuit board, however, it does not also disclose said first via extending from said first substrate surface to said second substrate surface of a core of said multi-layer printed circuit board with the first via passing through said first dielectric layer. Please keep in mind that claims 30-33 state an **additional ...** via wherein that via must extend through said metallic layer and that a **different** first via (claim 1) must also contact that same metallic layer and go through a first dielectric layer as well as a first substrate surface and a second substrate surface of a core substrate as stated in claims 20, and 21. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 20, 21, and 40 thru 44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 20, and 21, it is unclear how "the first via extends from said first substrate surface to said second substrate surface" when the "first via passing through said first dielectric layer" (claim 17) when the first dielectric layer is disposed on said first substrate surface of a polymeric circuit board.

Claims 40 thru 44 recite the limitation "the core" and "said multi-layer printed circuit board" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 44 recites the limitation "a patterned metallic layer" separately in lines 8, and 15 of said claim. It is unclear whether this is the same patterned metallic layer or two different patterned metallic layers. Appropriate clarification and/or correction are required.

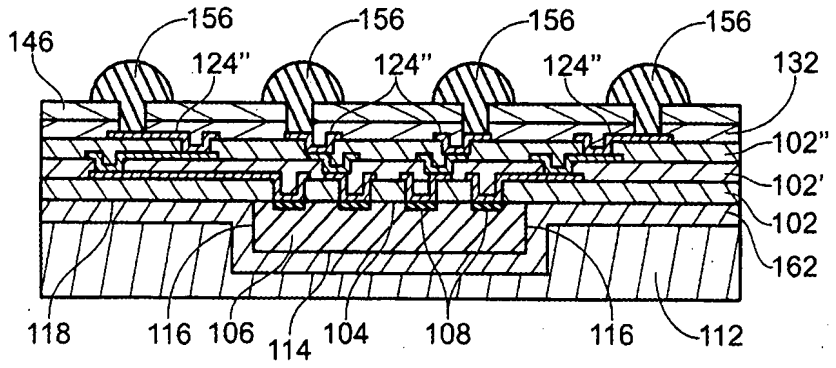
Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 17, 33, 34, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. 6,154,366 in view of Wojnarowski et al. 5,866,952 in view of Higashi et al. 6,861,284 B2. Ma discloses (see, for example, Fig. 2j) a package (multi-layer printed circuit board) comprising an encapsulation material (circuit board substrate) 112 having a first substrate surface and a second substrate surface, die (first integrated electronic component) 106, cavity, flex component (first dielectric layer) 102, conductive trace (metallic layer) 124, electrically conductive first via, element (second dielectric layer) 102', and electrically conductive second via.

Fig. 2j



Ma does not disclose the circuit board substrate being polymeric. However, Wojnarowski discloses (see, for example, FIG. 1(e)) an integrated module substrate comprising a chip 14, and substrate molding material (circuit board substrate) 24. In column 7, lines 50-62, Wojnarowski discloses the substrate molding material being polymers (polymeric). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the circuit board substrate being polymeric in order to have a material that adequately supports a die in a substrate form, and any overlying layers wherein the material is not prone to cracking.

Ma in view of Wojnarowski does not disclose a second electrically conductive via extending at one location. However, Higashi discloses (see, for example, Fig. 7) a substrate 10 comprising a wiring pattern (second electrically conductive via) 18 in a via hole. The wiring traverses multiple insulating layers. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second electrically conductive via extending at one location in order to lessen manufacture time, and save material.

Regarding claims 33, and 34, Ma discloses (see, for example, FIG. 1d) multiple conductive traces (at least one metal-lined via) 124. The multiple conductive traces transmit signals to the die.

Regarding claims 38, and 39, these claims contain product-by-process limitations (i.e. is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board (claim 38), and at a temperature of greater than about 600 C (claim 39)) that do not structurally differentiate the applicant's claimed structure from Ma in view of Wojnarowski in view of Higashi.

6. Claims 18, 20 thru 23, 27, 30, 36, 40, 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 as applied to claims 17, 33, 34, 38, and 39 and further in view of Miura et al. 5,565,706. Ma in view of Wojnarowski in view of Higashi does not disclose a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface. Miura discloses (see, for example, FIG. 6) a multi-layer package board (multi-layer printed circuit board) comprising a package board 46 having external output terminals (first metallic layer) 8 and external output terminals (second metallic layer) 28. It would have been obvious to one of ordinary skill in the art at the time of invention to have a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface in order to include external connections to the substrate such as voltages, metallizations, etc.

Regarding claims 20-23, see, for example, FIG. 6 wherein Miura discloses a via going through the package board 46 that connects the exteran louput terminals and other metal layers in the dielectric layers.

Regarding claim 27, see figures wherein Miura discloses external output terminals (conductive pad) 8 on top of the LSI 35.

Regarding claim 30, see FIG. 6 wherein Miura discloses one of the vias (at least one metal-lined via) 16 attached to LSI 33.

Regarding claim 36, see, for example, column 8, lines 25-28 wherein Miura discloses a capacitor.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 as applied to claims 17, 33, 34, 38, and 39 above, and further in view of Desai 5,739,188. Ma in view of Wojnarowski in view of Higashi does not disclose the multi-layer core substrate comprising at least two polymeric layers. However, Desai discloses (see, for example, column 3, lines 26-30) a multi layered product wherein the product comprises a substrate layer/cap layer (two polymeric layers). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the multi-layer core substrate comprising at least two polymeric layers in order to protect the substrate.

8. Claims 24, 26, 28, 29, 31, 32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 in view of Miura et al. '706 as applied to claims 18, 20-23, 27, 30, 36, 40, 41, and 43 above, and further in view of Marcinkiewicz et al. 5,241,456. Ma in view of Wojnarowski in view of Higashi in view of Miura does not disclose said exposed portion of said second substrate

surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity. However, Marcinkiewicz discloses (see, for example, FIG. 1) a structure 10 comprising a substrate 12, and chip (second integrated electronic component) 36. Having the chip in the same substrate creates a multichip device that saves space and provides interconnection between two chips. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity in order to create a multichip device that saves space and provides interconnection between two chips.

Regarding claim 28, see, for example, FIG. 1 wherein Marcinkiewicz discloses contact pad (conductive pad) 38.

Regarding claim 29, see, for example, FIG. 1 wherein Miura discloses contact pad (conductive pad) 8 on top of the LSI 35.

Regarding claim 44, Miura in view of Wojnarowski in view of Higashi in view of Miura does not disclose a third dielectric layer disposed on said second side of said substrate. However, Marcinkiewicz discloses (see, for example, FIG. 1) a substrate 12, and dielectric layer (third dielectric layer) 52. The dielectric layer protects the bottom surface of the substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a third dielectric layer disposed on said second side of said substrate in order to protect the bottom of the substrate.

9. Claims 37, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 in view of Miura et al. '706 as applied to claims 18, 20-23, 27, 30, 36, 40, 41, and 43 above, and further in view of Miyazawa et al. 5,953,619. Ma in view of Wojnarowski in view of Higashi in view of Miura does not disclose said capacitor comprising a perovskite capacitance material. However, Miyazawa discloses (see, for example, column 1, lines 27-35) that a perovskite crystal structure has a high dielectric constant. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said capacitor comprising a perovskite capacitance material in order to have a higher dielectric constant in the same area.

Response to Arguments

10. Applicant's arguments with respect to claims 17-24, 26-34, and 36-44 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
May 29, 2007

EUGENE LEE
PRIMARY EXAMINER